
# BUK9K31-100L

## Dual N-Channel 100V, 31 mOhm logic level MOSFET in LFPAK56D

17 December 2024 Product data sheet

## 1. General description

Dual N-channel logic level MOSFET in an LFPAK56D (Dual Power-SO8) package. This product has been designed and qualified to AEC-Q101 standard for use in high performance automotive applications.

## 2. Features and benefits

- Dual MOSFET – two silicon dies in one LFPAK56D package for significant space saving
- Trench12 MOSFET technology
- Efficient switching with soft body-diode recovery
- Automotive qualified to AEC-Q101 at 175 °C
- Side-wettable flanks for robust solder joints and automatic optical inspection

## 3. Applications

- 12 V 24 V and 48 V automotive systems
- Motor, lighting, and solenoid control
- Transmission control
- LED lighting
- Circuit protection

## 4. Quick reference data

**Table 1. Quick reference data**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Limiting values FET1 and FET2** | | | | | | | |
| $V_{DS}$ | drain-source voltage | 25 °C ≤ $T_j$ ≤ 175 °C | | - | - | 100 | V |
| $I_D$ | drain current | $V_{GS}$ = 10 V; $T_{mb}$ = 25 °C; Fig. 2 | [1] | - | - | 24 | A |
| $P_{tot}$ | total power dissipation | $T_{mb}$ = 25 °C; Fig. 1 | | - | - | 43 | W |
| **Static characteristics FET1 and FET2** | | | | | | | |
| $R_{DSon}$ | drain-source on-state resistance | $V_{GS}$ = 10 V; $I_D$ = 5 A; $T_j$ = 25 °C; Fig. 11 | | 13.4 | 25 | 31.7 | mΩ |
| **Dynamic characteristics FET1 and FET2** | | | | | | | |
| $Q_{GD}$ | gate-drain charge | $I_D$ = 5 A; $V_{DS}$ = 50 V; $V_{GS}$ = 5 V; $T_j$ = 25 °C; Fig. 13; Fig. 14 | | 0.8 | 2.8 | 6 | nC |

[1] 24 A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

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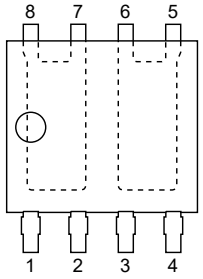
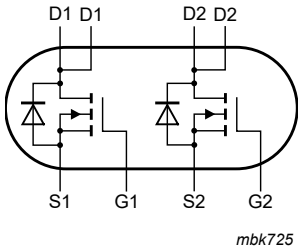
# 5. Pinning information

**Table 2. Pinning information**

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|---|---|---|---|---|
| 1 | S1 | source1 |  **LFPAK56D; Dual LFPAK (SOT1205)** |  |
| 2 | G1 | gate1 | | |
| 3 | S2 | source2 | | |
| 4 | G2 | gate2 | | |
| 5 | D2 | drain2 | | |
| 6 | D2 | drain2 | | |
| 7 | D1 | drain1 | | |
| 8 | D1 | drain1 | | |

# 6. Ordering information

**Table 3. Ordering information**

| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| BUK9K31-100L | LFPAK56D; Dual LFPAK | plastic, single ended surface mounted package (LFPAK56D); 8 leads | SOT1205 |

# 7. Marking

**Table 4. Marking codes**

| Type number | Marking code |
|---|---|
| BUK9K31-100L | 9311HL |

# 8. Limiting values

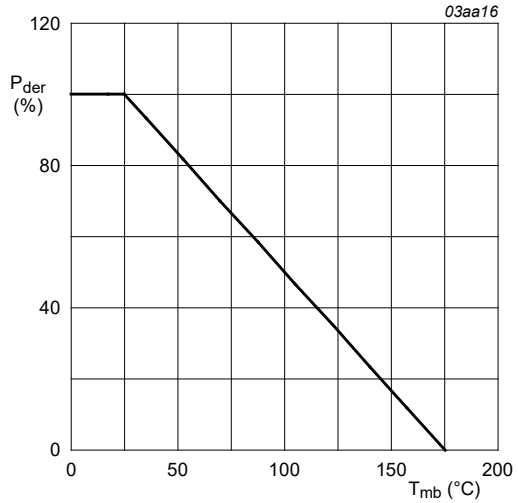
**Table 5. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134). Tj = 25 °C unless otherwise stated.*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| **Limiting values FET1 and FET2** | | | | | | |
| $V_{DS}$ | drain-source voltage | 25 °C ≤ $T_j$ ≤ 175 °C | | - | 100 | V |
| $V_{GS}$ | gate-source voltage | | [1] | -20 | 20 | V |
| $P_{tot}$ | total power dissipation | $T_{mb}$ = 25 °C; Fig. 1 | | - | 43 | W |
| $I_D$ | drain current | $V_{GS}$ = 10 V; $T_{mb}$ = 25 °C; Fig. 2 | [2] | - | 24 | A |
| | | $V_{GS}$ = 10 V; $T_{mb}$ = 100 °C; Fig. 2 | | - | 17 | A |
| $I_{DM}$ | peak drain current | pulsed; $t_p$ ≤ 10 µs; $T_{mb}$ = 25 °C; Fig. 3 | | - | 98 | A |
| $T_{stg}$ | storage temperature | | | -55 | 175 | °C |
| $T_j$ | junction temperature | | | -55 | 175 | °C |
| **Source-drain diode FET1 and FET2** | | | | | | |
| $I_S$ | source current | $T_{mb}$ = 25 °C | | - | 24 | A |
| $I_{SM}$ | peak source current | pulsed; $t_p$ ≤ 10 µs; $T_{mb}$ = 25 °C | | - | 98 | A |

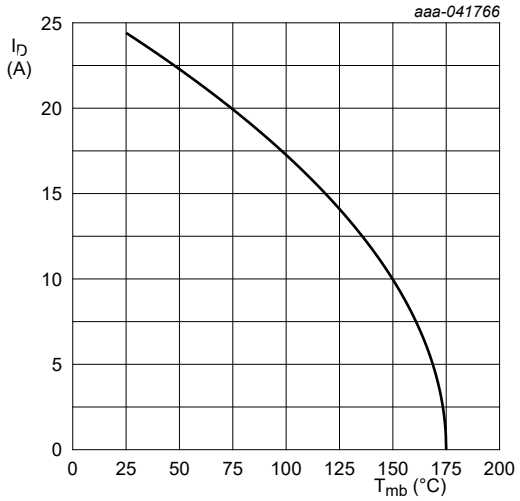
| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| **Avalanche ruggedness FET1 and FET2** | | | | | | |
| $E_{DS(AL)S}$ | non-repetitive drain-source avalanche energy | $I_D$ = 8.3 A; $V_{sup} \leq$ 100 V; $R_{GS}$ = 50 Ω; $V_{GS}$ = 5 V; $T_{j(init)}$ = 25 °C; unclamped; $t_{AL}$ = 75 µs; Fig. 4 | [3] [4] | - | 40.7 | mJ |
| $I_{AS}$ | non-repetitive avalanche current | $V_{sup}$ = 100 V; $V_{GS}$ = 5 V; $T_{j(init)}$ = 25 °C; $R_{GS}$ = 50 Ω; Fig. 4 | [3] [4] | - | 8.3 | A |

[1] Refer to application note AN90001 for further information.
[2] 24 A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.
[3] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
[4] Refer to application note AN10273 for further information.



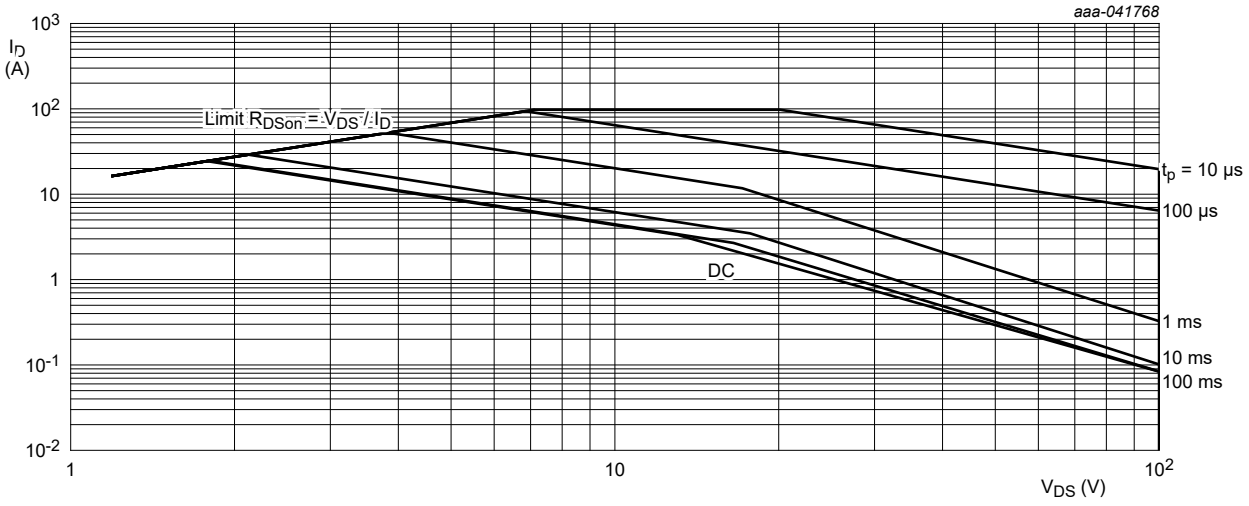

$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

**Fig. 1. Normalized total power dissipation as a function of mounting base temperature**



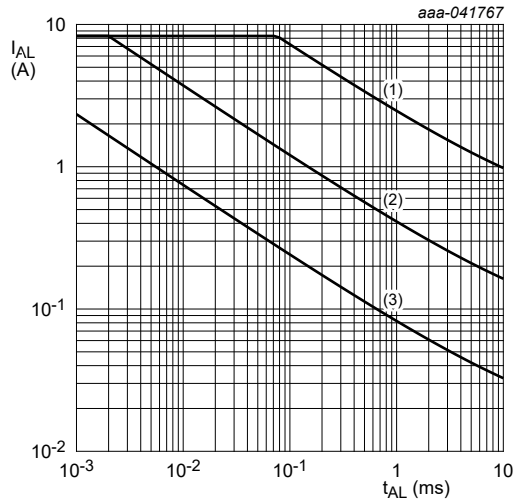

$V_{GS} \geq 10$ V
24 A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

**Fig. 2. Continuous drain current as a function of mounting base temperature, FET1 and FET2**




$T_{mb}$ = 25 °C; $I_{DM}$ is a single pulse

**Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage, FET1 and FET2**




(1) $T_{j\ (init)}$ = 25 °C; (2) $T_{j\ (init)}$ = 150 °C; (3) Repetitive Avalanche

**Fig. 4. Avalanche rating; avalanche current as a function of avalanche time, FET1 and FET2**

# 9. Thermal characteristics

**Table 6. Thermal characteristics**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $R_{th(j\text{-}mb)}$ | thermal resistance from junction to mounting base | Fig. 5 | | - | 2.11 | 3.45 | K/W |

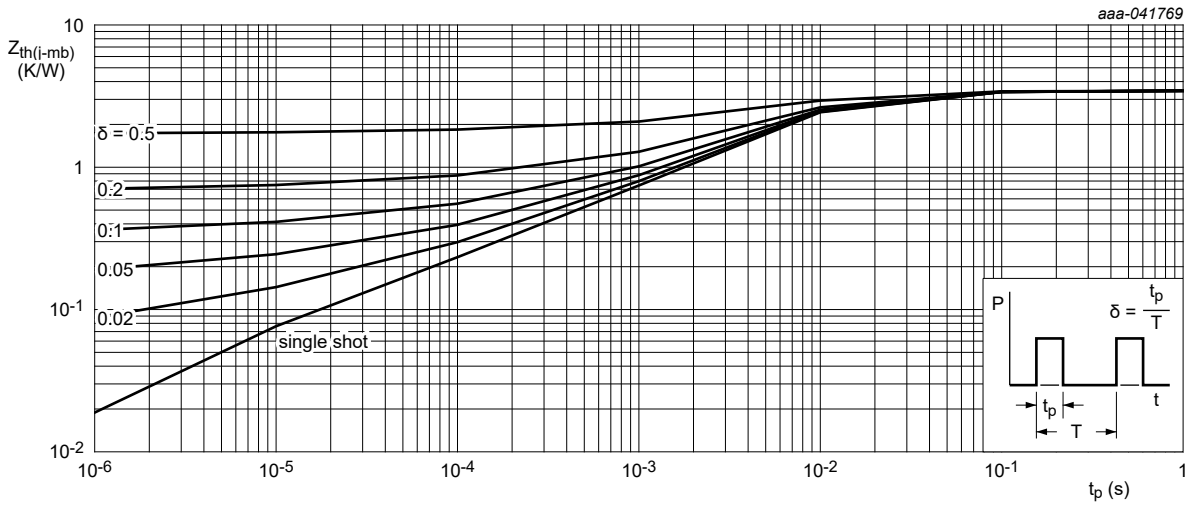


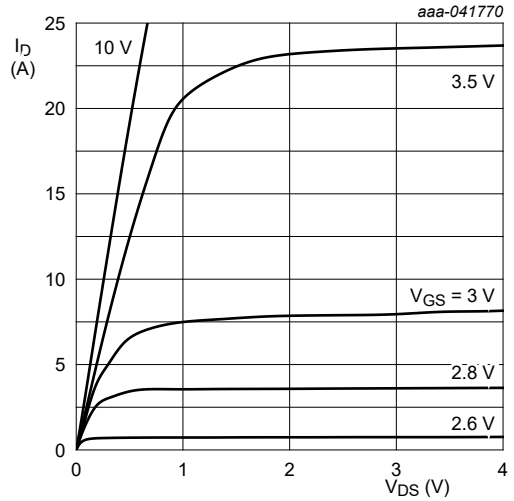

**Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration, FET1 and FET2**

# 10. Characteristics

**Table 7. Characteristics**

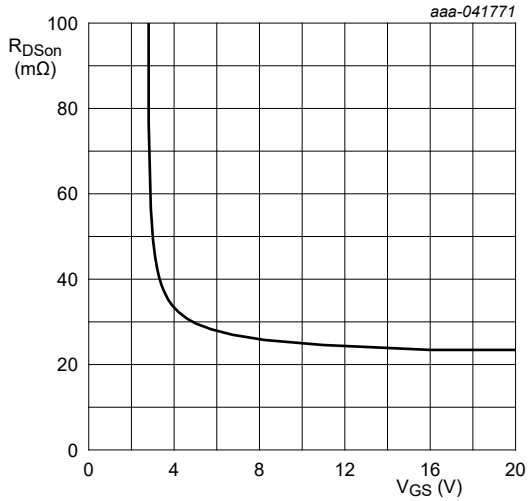
| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Static characteristics FET1 and FET2** | | | | | | | |
| $V_{(BR)DSS}$ | drain-source breakdown voltage | $I_D$ = 250 µA; $V_{GS}$ = 0 V; $T_j$ = 25 °C | | 100 | 118.3 | - | V |
| | | $I_D$ = 250 µA; $V_{GS}$ = 0 V; $T_j$ = -40 °C | | 92 | 112 | - | V |
| | | $I_D$ = 250 µA; $V_{GS}$ = 0 V; $T_j$ = -55 °C | | 90 | 110 | - | V |
| $V_{GS(th)}$ | gate-source threshold voltage | $I_D$ = 0.05 mA; $V_{DS}$=$V_{GS}$; $T_j$ = 25 °C; Fig. 9; Fig. 10 | | 1.4 | 1.7 | 2.05 | V |
| | | $I_D$ = 0.05 mA; $V_{DS}$=$V_{GS}$; $T_j$ = 175 °C; Fig. 10 | | 0.5 | - | - | V |
| | | $I_D$ = 0.05 mA; $V_{DS}$=$V_{GS}$; $T_j$ = -55 °C; Fig. 10 | | - | - | 2.3 | V |
| $I_{DSS}$ | drain leakage current | $V_{DS}$ = 100 V; $V_{GS}$ = 0 V; $T_j$ = 25 °C | | - | 0.006 | 1 | µA |
| | | $V_{DS}$ = 100 V; $V_{GS}$ = 0 V; $T_j$ = 125 °C | | - | 2 | 100 | µA |
| | | $V_{DS}$ = 100 V; $V_{GS}$ = 0 V; $T_j$ = 175 °C | | - | 25 | 500 | µA |
| $I_{GSS}$ | gate leakage current | $V_{GS}$ = 20 V; $V_{DS}$ = 0 V; $T_j$ = 25 °C | | - | 2 | 100 | nA |
| | | $V_{GS}$ = -20 V; $V_{DS}$ = 0 V; $T_j$ = 25 °C | | - | 2 | 100 | nA |
| $R_{DSon}$ | drain-source on-state resistance | $V_{GS}$ = 10 V; $I_D$ = 5 A; $T_j$ = 25 °C; Fig. 11 | | 13.4 | 25 | 31.7 | mΩ |
| | | $V_{GS}$ = 10 V; $I_D$ = 5 A; $T_j$ = 100 °C; Fig. 12 | | 19.7 | 38.5 | 51 | mΩ |
| | | $V_{GS}$ = 10 V; $I_D$ = 5 A; $T_j$ = 125 °C; Fig. 12 | | 21.5 | 42.3 | 56.3 | mΩ |
| | | $V_{GS}$ = 10 V; $I_D$ = 5 A; $T_j$ = 175 °C; Fig. 12 | | 26.2 | 53 | 72.5 | mΩ |
| | | $V_{GS}$ = 4.5 V; $I_D$ = 5 A; $T_j$ = 25 °C; Fig. 11 | | 21.7 | 31 | 47 | mΩ |
| | | $V_{GS}$ = 4.5 V; $I_D$ = 5 A; $T_j$ = 100 °C; Fig. 12 | | 32 | 47.7 | 75.5 | mΩ |
| | | $V_{GS}$ = 4.5 V; $I_D$ = 5 A; $T_j$ = 125 °C; Fig. 12 | | 34.8 | 52.4 | 83.5 | mΩ |
| | | $V_{GS}$ = 4.5 V; $I_D$ = 5 A; $T_j$ = 175 °C; Fig. 12 | | 42.4 | 65.7 | 107.6 | mΩ |
| $R_G$ | gate resistance | f = 1 MHz; $T_j$ = 25 °C | | 0.8 | 1.6 | 3.2 | Ω |
| **Dynamic characteristics FET1 and FET2** | | | | | | | |
| $Q_{G(tot)}$ | total gate charge | $I_D$ = 5 A; $V_{DS}$ = 50 V; $V_{GS}$ = 5 V; $T_j$ = 25 °C; Fig. 13; Fig. 14 | | 5.4 | 10.9 | 16.3 | nC |
| | | $I_D$ = 5 A; $V_{DS}$ = 50 V; $V_{GS}$ = 10 V; $T_j$ = 25 °C; Fig. 13; Fig. 14 | | 10.3 | 20.7 | 31 | nC |
| $Q_{GS}$ | gate-source charge | $I_D$ = 5 A; $V_{DS}$ = 50 V; $V_{GS}$ = 5 V; $T_j$ = 25 °C; Fig. 13; Fig. 14 | | 2.2 | 3.7 | 5.2 | nC |
| $Q_{GD}$ | gate-drain charge | | | 0.8 | 2.8 | 6 | nC |
| $V_{GS(pl)}$ | gate-source plateau voltage | $I_D$ = 5 A; $V_{DS}$ = 50 V; $T_j$ = 25 °C; Fig. 13; Fig. 14 | | - | 2.8 | - | V |
| $C_{iss}$ | input capacitance | $V_{DS}$ = 25 V; $V_{GS}$ = 0 V; f = 1 MHz; $T_j$ = 25 °C; Fig. 15 | | 832 | 1386 | 1940 | pF |
| $C_{oss}$ | output capacitance | | | 196 | 326 | 521 | pF |
| $C_{rss}$ | reverse transfer capacitance | | | 12 | 30 | 49 | pF |

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $t_{d(on)}$ | turn-on delay time | $V_{DS}$ = 50 V; $R_L$ = 10 Ω; $V_{GS}$ = 5 V; $R_{G(ext)}$ = 5 Ω; $T_j$ = 25 °C | | - | 9.7 | - | ns |
| $t_r$ | rise time | | | - | 9.2 | - | ns |
| $t_{d(off)}$ | turn-off delay time | | | - | 14.5 | - | ns |
| $t_f$ | fall time | | | - | 9.1 | - | ns |
| **Source-drain diode FET1 and FET2** | | | | | | | |
| $V_{SD}$ | source-drain voltage | $I_S$ = 5 A; $V_{GS}$ = 0 V; $T_j$ = 25 °C; Fig. 16 | | - | 0.83 | 1 | V |
| $t_{rr}$ | reverse recovery time | $I_S$ = 5 A; $dI_S/dt$ = -100 A/µs; $V_{GS}$ = 0 V; $V_{DS}$ = 50 V; $T_j$ = 25 °C; Fig. 17 | | - | 42 | - | ns |
| $Q_r$ | recovered charge | | | - | 29 | - | nC |



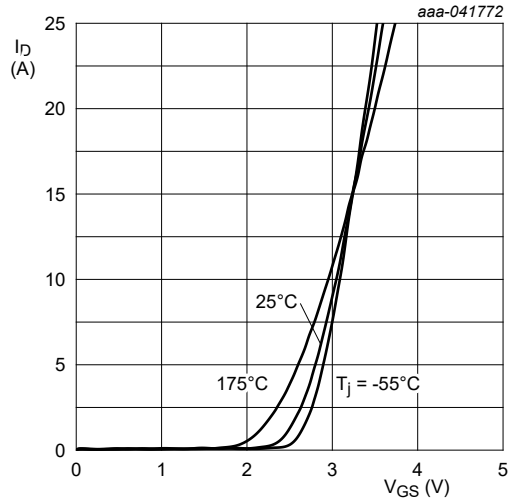

$T_j$ = 25 °C

**Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values, FET1 and FET2**



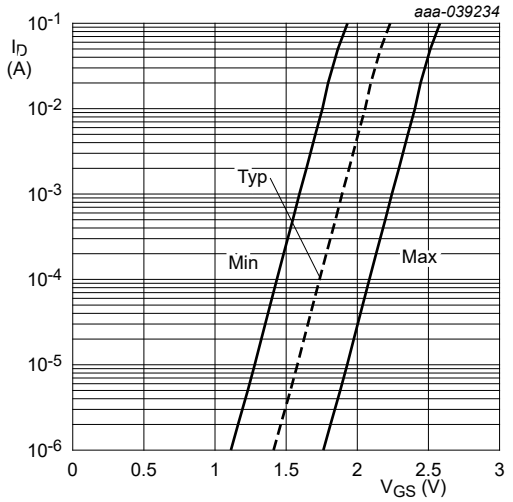

$T_j$ = 25 °C; $I_D$ = 5 A

**Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values, FET1 and FET2**



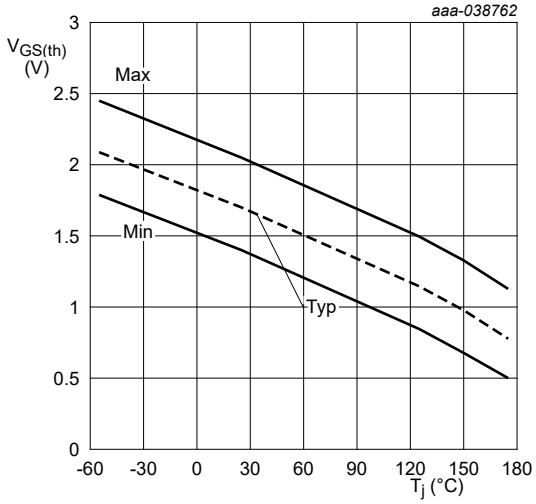

$V_{DS}$ = 8 V

**Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values, FET1 and FET2**



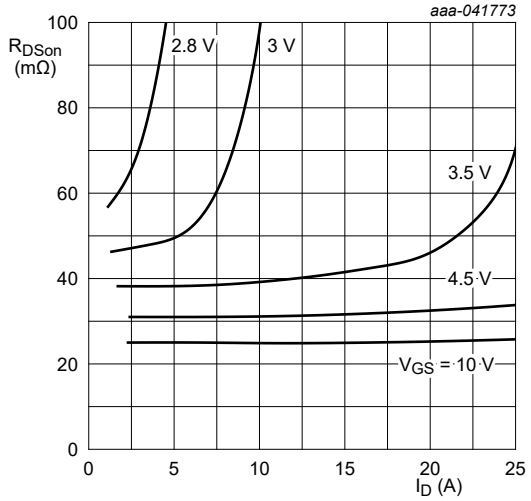

$T_j$ = 25 °C; $V_{DS}$ = 5 V

**Fig. 9. Sub-threshold drain current as a function of gate-source voltage, FET1 and FET2**



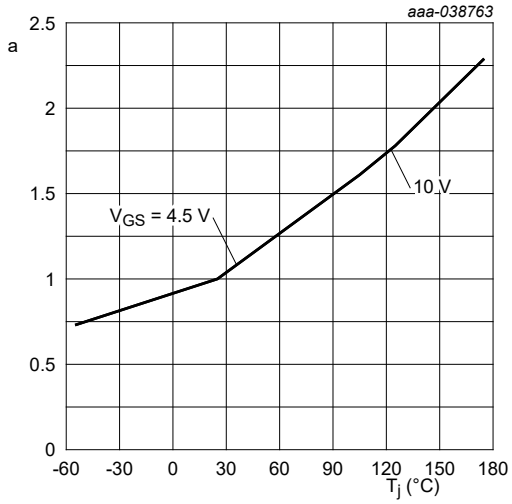

$I_D$ = 0.05 mA ; $V_{DS}$ = $V_{GS}$

**Fig. 10. Gate-source threshold voltage as a function of junction temperature, FET1 and FET2**



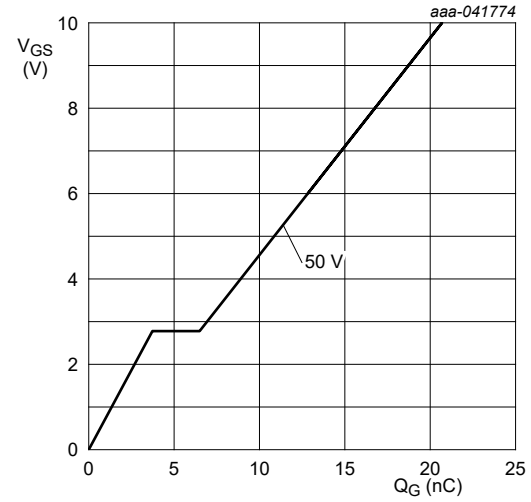

$T_j$ = 25 °C

**Fig. 11. Drain-source on-state resistance as a function of drain current; typical values, FET1 and FET2**




$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

**Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature, FET1 and FET2**




$T_j$ = 25 °C; $I_D$ = 5 A

**Fig. 13. Gate-source voltage as a function of gate charge; typical values, FET1 and FET2**

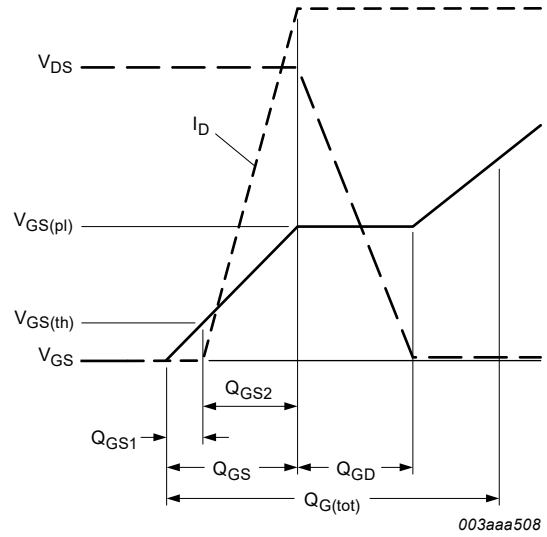
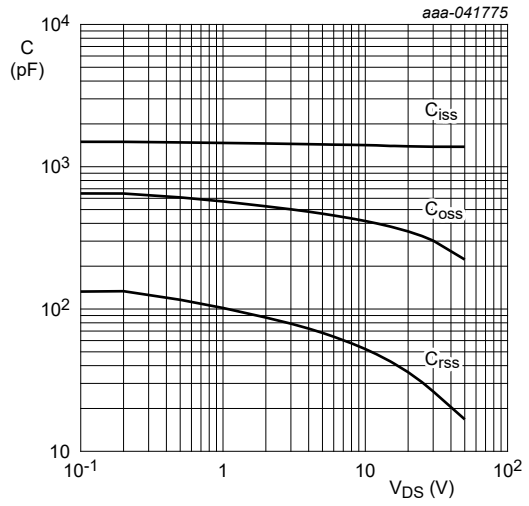
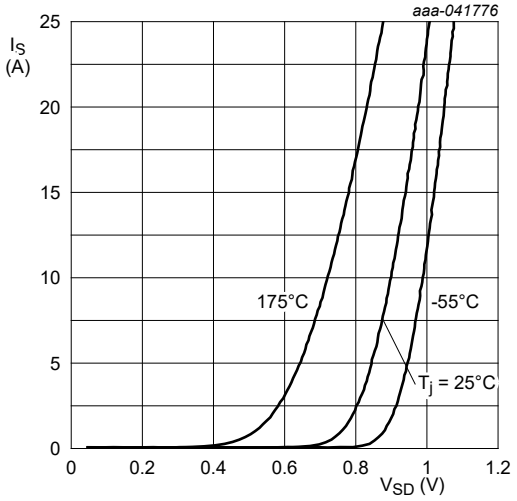



**Fig. 14. Gate charge waveform definitions**




$V_{GS}$ = 0 V; f = 1 MHz

**Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values, FET1 and FET2**




$V_{GS}$ = 0 V

**Fig. 16. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values, FET1 and FET2**

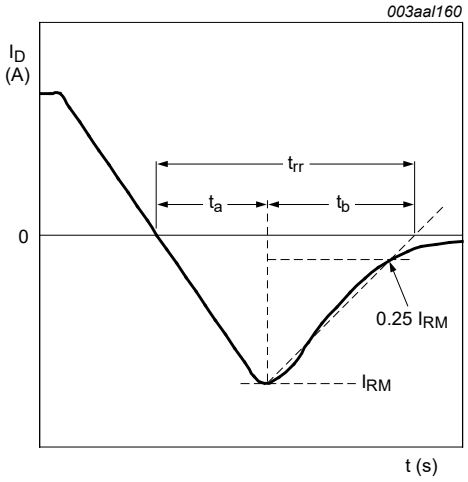
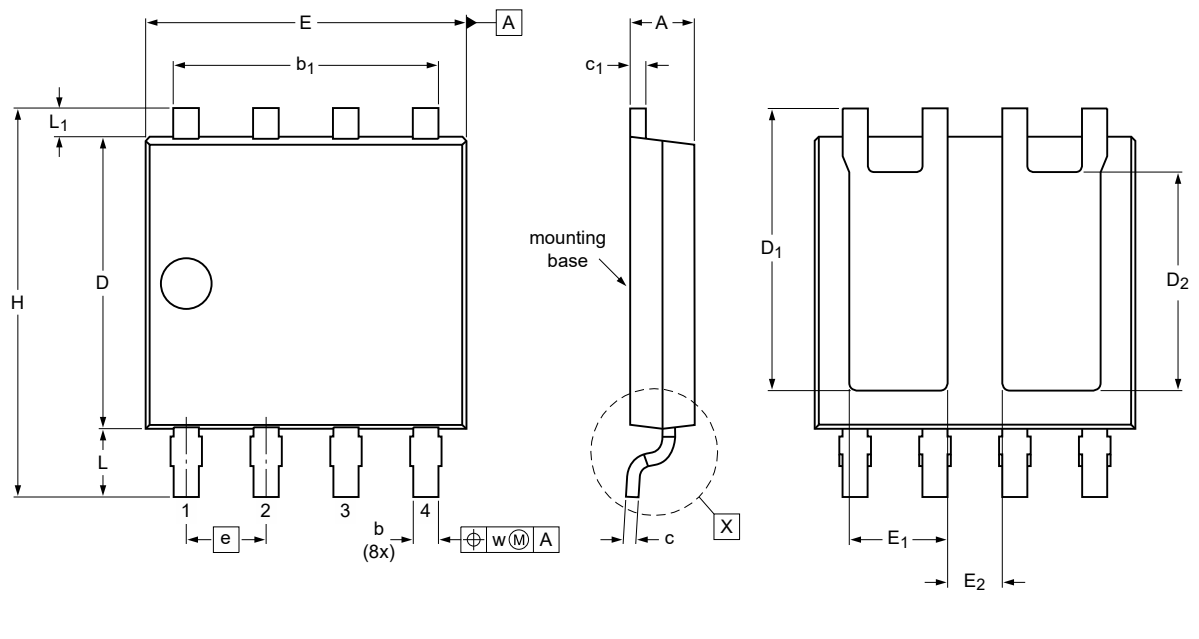



**Fig. 17. Reverse recovery timing definition**

# 11. Package outline

**Plastic single ended surface mounted package LFPAK56D; 8 leads** **SOT1205**




Dimensions

| Unit | | A | $A_1$ | b | $b_1$ | c | $c_1$ | $D^{(1)}$ | $D_1{}^{(1)}$ | $D_2$ (ref) | $E^{(1)}$ | $E_1{}^{(1)}$ | $E_2$ | e | H | L | $L_1$ | $L_p$ | w | y | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | max | 1.05 | 0.1 | 0.50 | 4.4 | 0.25 | 0.30 | 4.70 | 4.55 | 3.5 | 5.30 | 1.8 | 0.85 | | 6.2 | 1.3 | 0.55 | 0.85 | | | 8° |
| | nom | | | | | | | | | | | | | 1.27 | | | | | 0.25 | 0.1 | |
| | min | 1.02 | 0.0 | 0.35 | 4.1 | 0.19 | 0.24 | 4.45 | 4.35 | 3.4 | 4.95 | 1.6 | 0.60 | | 5.9 | 0.8 | 0.30 | 0.40 | | | 0° |

Note
1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

*sot1205_po*

| Outline version | References | | | | European projection | Issue date |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT1205 | | | | | | ~~14-08-21~~ 14-10-28 |

**Fig. 18. Package outline LFPAK56D; Dual LFPAK (SOT1205)**

# 12. Legal information

## Data sheet status

| Document status [1][2] | Product status [3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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For sales office addresses, please send an email to: salesaddresses@nexperia.com
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